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10EC751

Seventh Semester B.E. Degree Examination, June/July 2014
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is Digital Signal Processing? Explain the issues to be considered in designing and implementing a DSP system. **(09 Marks)**

b. Write a MATLAB code for design an FIR filter using Parks-McClellen method. **(05 Marks)**

c. Explain the decimation and interpolation processes with an example. **(06 Marks)**

2 a. What is role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter with a diagram. **(06 Marks)**

b. Identify the addressing modes of the operands in each of the following instructions and their operation:
(i) ADD B (ii) ADD 5678h (iii) ADD + *addrreg (iv) ADD *addrreg, offsetreg – **(08 Marks)**

c. Explain the purpose of a program sequencer with a block diagram. **(06 Marks)**

3 a. Describe the multiplier / adder unit of TMS320C54× processor with a neat block diagram. **(06 Marks)**

b. Describe any four data addressing modes of TMS320C54XX DSP with examples. **(08 Marks)**

c. Assuming current contents of AR_3 to be 200h, what will be its contents after each of the following TMS320C54× addressing modes is used? Assume that the contents of AR0 are 20h.
(i) * AR_3 +0 (ii) * AR_3 + (iii) *+AR_3(40h) **(06 Marks)**

4 a. Describe the operation of the following instructions of TMS320C54× processor with an example :
(i) MAC (ii) RPT (iii) MPY **(06 Marks)**

b. Write a program to find the sum of a series of signed numbers stored at successive locations in the data memory and place the result in the accumulator A
ie., $A = \sum_{G=410h}^{41fh} dmad(i)$ **(06 Marks)**

c. Describe the operation of hardware timer with a neat diagram. **(08 Marks)**

PART – B

5 a. Describe the importance of Q-notation in DSP algorithm implementation, with examples.

b. What are the values represented by 16-bit fixed point number N = 4000h in Q15, Q10, Q7 notations? **(10 Marks)**

c. Explain how the FIR filter algorithms can be implemented using TMS320C54XX processor. **(10 Marks)**

6 a. Explain a general DITFFT butterfly in place computation structure. **(04 Marks)**
b. Determine the no. of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT. **(06 Marks)**
c. Explain how the bit-reserved index generation can be done in 8-point FFT. Also write a TMS320C54XX program for 8-point DITFFT bit reversed index generation. **(10 Marks)**

7 a. Explain the memory interface block diagram for the TMS320C54XX processor. **(06 Marks)**
b. Draw the I/O interface timing diagram for read-write-read sequence of operation. **(06 Marks)**
c. What are interrupts? How interrupts are handled by the C54XX DSP processors. **(08 Marks)**

8 a. Draw the block diagram of PCM3002 CODEC and explain about it. **(10 Marks)**
b. With the help of block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(10 Marks)**

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